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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,159	09/12/2003	KUN-HONG CHEN	9894-US-PA	2158

31561 7590 02/27/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER

PHAM, LONG

ART UNIT PAPER NUMBER

2814

DATE MAILED: 02/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/605,159

Applicant(s)

CHEN, KUN-HONG

Examiner

Long Pham

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: ____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 4, 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Yu (US '104).

With respect to claim 1, AAPA teaches a polysilicon thin film transistor, comprising:

a substrate 100, fig. 1;

a poly-island layer 102 over the substrate, wherein the poly-island layer having:

a channel region 102a, and

a doped source/drain region 102b;

a gate 106 over the channel region of the poly-island layer;

a gate insulating film 104 between the gate and the poly-island layer, the insulating film further comprising:

a silicon oxide layer 104 covering the poly-island layer; and

an inter-layer dielectric 108 or 109 over the gate and the gate insulating film.

AAPA teaches that the gate insulating film comprises of a silicon oxide layer but fails to teach that the gate insulating film comprises of a silicon nitride layer formed on silicon oxide layer.

Yu teaches that a gate insulating film comprises silicon oxide layer formed on a silicon nitride layer provides performance, reliability, and manufacturability. See col. 3, lines 17-20.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Yu's teaching into the device of AAPA to obtain the above advantages.

With respect claims 4 and 5, AAPA does not explicitly teach that the source/drain region is doped n or p type.

However, it is inherent that the source/drain region must be either doped n or p type for the device to be functional.

With respect to claim 6, AAPA further teaches that the poly-island layer further includes a lightly doped drain 102c between the channel region and the doped source/drain region.

3. Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Yu (US '104).

With respect to claims 2 and 3, AAPA in combination with Yu fail to teach the ranges for the thicknesses of the silicon oxide and silicon nitride layer of the gate insulating layer.

However, it would have been obvious to one of ordinary skill in the art of making semiconductor devices to determine the workable or optimal ranges for thicknesses of the silicon oxide and silicon nitride layers of the gate insulating layer through routine experimentation and optimization to obtain optimal or desired device performance because the thicknesses are result-effective variables and there is no evidence indicating that the thicknesses critical or produce any unexpected results and it has been held that it is not inventive to discover the optimum or

workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Yu (US '104).

With respect to claim 7, AAPA in combination with Yu fail to teach forming a buffer layer on the substrate before the formation of a device.

However, the formation of a buffer layer on a substrate prior to the formation of a device is well-known to one skilled in the semiconductor art.

5. Claims 8, 11, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Yu (US '104).

With respect to claim 8, AAPA teaches a polysilicon thin film transistor, comprising:

a gate 106;

a poly-island layer 102 under the gate, wherein the poly-island layer further includes a channel region 102a under the gate and a doped source/drain region 102b on each side of the channel region;

a gate insulating film 104 between the gate and poly-island layer, wherein the gate insulating film includes a silicon oxide layer 104, wherein the silicon oxide layer covers the poly-island layer;

a first inter-layer dielectric 108 over the gate and the gate insulating film; source/drain contact metal 110 embedded between the first inter-layer dielectric and the gate insulating film on each side of the gate, wherein the source/drain contact metal is electrically connected to the doped source/drain region; and

a second inter-layer dielectric 109 covering the first inter-layer dielectric and the source/drain contact metal.

AAPA teaches that the gate insulating film comprises of a silicon oxide layer but fails to teach that the gate insulating film comprises of a silicon nitride layer formed on silicon oxide layer.

Yu teaches that a gate insulating film comprises silicon oxide layer formed on a silicon nitride layer provides performance, reliability, and manufacturability. See col. 3, lines 17-20.

It would have been obvious to one of ordinary skill in the art of making semiconductor devices to incorporate Yu's teaching into the device of AAPA to obtain the above advantages.

With respect claims 11 and 12, AAPA does not explicitly teach that the source/drain region is doped n or p type.

However, it is inherent that the source/drain region must be either doped n or p type for the device to be functional.

With respect to claim 13, AAPA further teaches that the poly-island layer further includes a lightly doped drain 102c between the channel region and the doped source/drain region.

6. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in combination with Yu (US '104).

With respect to claim 14, AAPA in combination with Yu fail to teach forming a buffer layer on the substrate before the formation of a device.

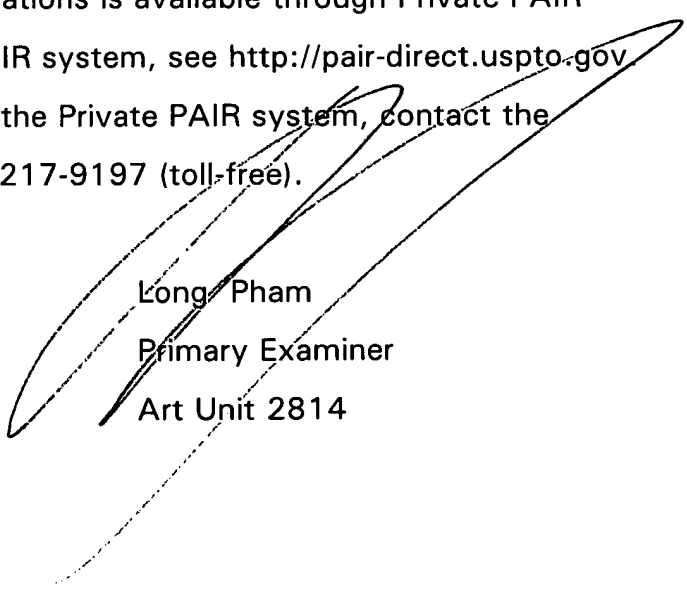
However, the formation of a buffer layer on a substrate prior to the formation of a device is well-known to one skilled in the semiconductor art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Long Pham whose telephone number is 703-308-1092. The examiner can normally be reached on M-F, 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 703-308-4918. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Long Pham
Primary Examiner
Art Unit 2814

LP